Effective Teaching of the Physical Design of Integrated Circuits Using Educational Tools

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***Abstract*—This paper presents the strategies used for effective teaching and skill development in integrated circuit (IC) design using project-based learning (PBL) methodologies. It presents the contexts in which these strategies are applied to IC design courses at the University of South Australia, Adelaide, Australia, and the National Institute of Applied Science (INSA), Toulouse, France. Collaborations among the faculty members of the two institutions have produced a set of learning resources and design tools to support the development of industry-relevant design skills and lifelong learning skills. At the pedagogical level, the emphasis is on the development of practical circuit design, critical thinking, and problem-solving skills rather than the mastery of complex circuit design tools. The courses enable students to learn about the most recent technological developments and their implications, using a set of user-friendly tools. The PBL methodologies, intuitive design tools, and latest technology models have consistently produced high levels of student satisfaction with the overall quality of the courses at the two institutions.**

***Index Terms*—Educational technology, electronics engineering education, integrated circuit (IC) design, project-based learning (PBL).**

I. Introduction

THE past few years have seen the introduction of nanoscale technologies for industrial production of high-performance integrated circuits (ICs) [1]–[7]. Each technology scaling is characterized by a number of changes in the IC manufacturing process. The most evident changes are the decrease in layout pattern sizes such as the gate length. The processing in a new technology node also involves steps to improve the carrier mobility and the field effect beneath the gate as well as to reduce leakage currents [8], [9]. Consequently, technology scaling impacts upon the operation of the ICs by improving switching speed, signal transport, and reduced dc consumption and operating voltages [4]–[11]. Shifting to a new technology node has an impact upon the design methodology and requires improved technology models and tools to accurately predict the performances of the circuits [12]. The international roadmap for ICs [13] gives a prospective vision of the evolution of IC technology for the next 15 years, showing how future technology nodes (22, 18, 7 nm) are expected to push the limits of CMOS technology further. Engineering students need to be abreast of the rapid changes in technology and design practices. Courses in IC design must also aim to equip students with the skills of independent learning and lifelong learning. Due to time constraints in a semester-long course, it is often not feasible both to introduce students to complex commercial design tools and also expect them to develop practical circuit design skills and independent learning skills.

This paper presents project-based approaches to teaching adopted in two institutions in Australia and France, aimed at actively engaging students in stimulating learning experiences that help them develop both chip design skills using the latest semiconductor technologies and independent and lifelong learning abilities. The student cohorts in these two institutions differ in terms of their previous educational experience, background knowledge, and diversity. The project-based approaches at the University of South Australia (UniSA), Adelaide, Australia, and the National Institute of Applied Science (INSA), Toulouse, France, are tailored accordingly to maximize the learning outcomes of the two cohorts. Intuitive educational tools have been used to develop project-based learning (PBL) methodologies, which have achieved high levels of student satisfaction. Section II presents the recent developments in CMOS technology. Section III presents the recent educational developments and teaching challenges. Section IV illustrates the proposed design flow and associated tools. In Section V, examples of PBL at the two institutions are given along with descriptions of the skills developed. Section VI presents anonymous evaluation of the courses by students and the feedback received from peers. Section VII concludes the paper.

II. Developments in CMOS Technology

A. General Trends

With CMOS being the most dominant very large scale integration (VLSI) technology to date, it is useful to begin by looking at the developments in this technology and prospective future developments. The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area (Fig. 1). The 32-nm CMOS technology enables designs containing one billion devices on a chip (system-on-chip, SoC), or stacked dies and

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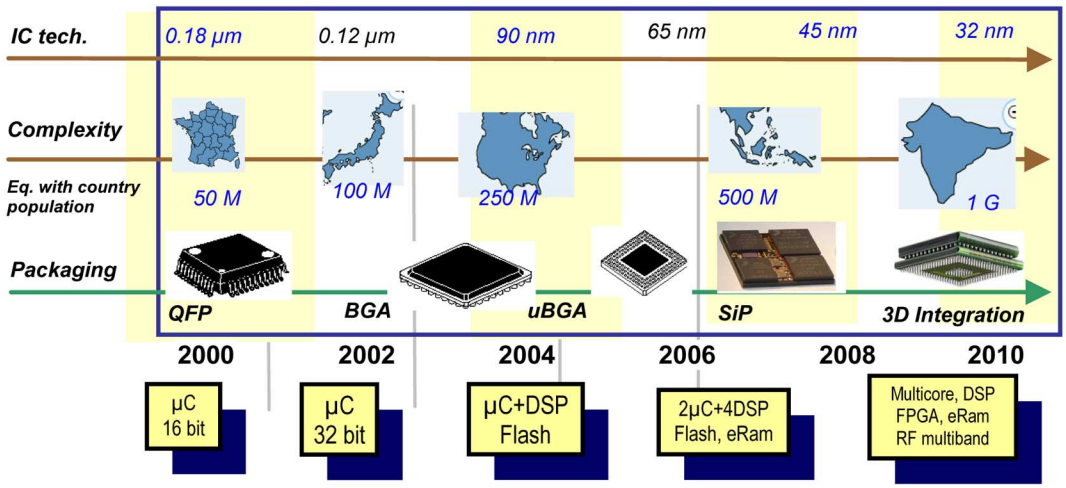

Fig. 1. More and more complex ICs.

TABLE I
TECHNOLOGICAL EVOLUTION AND FORECAST UP TO 2013 [13]

Key parameter	180 nm	90 nm	65 nm	45 nm	32 nm	22 nm	18 nm
First production	1999	2003	2005	2007	2009	2011	2013
Gate length	130 nm	50 nm	35 nm	30 nm	20 nm	15 nm	12 nm
Gate material & dielectric	Poly SiO_2	Poly SiO_2	Poly SiON	Metal High K	Metal High K	Dual gate?	Dual gate?
Atoms stacked on the gate oxide	10	8	6	5	5	5	5
Kgates per mm^2	100	350	500	900	1500	2800	4500
Memory point (μ^2)	4.5	1. 3	0.6	0.3	0.15	0.08	0.08

packages forming systems-in-packages, with typically multicore processors, parallel digital signal processors (DSPs), field programmable gate arrays (FPGAs), embedded RAM, as well as wireless communication capabilities in a single chip.

Table I gives an overview of the key parameters for technology nodes from 180 nm, introduced in 1999, down to 18 nm, which is supposed to be in production around 2013. The physical gate length is slightly smaller than the technological node, as illustrated in Fig. 2. The gate material has long been polysilicon, with silicon dioxide (SiO_2) as the insulator between the gate and the channel. The thinner the gate oxide, the higher the transistor current and the switching speed. SiO_2 has been continually scaled down over the last decade and reached a physical limit of five atomic layers in the 45-nm CMOS technology [5], [17]. With this technology, new materials such as metal gates together with high-permittivity gate oxide have been introduced [1]–[5], [14], [15].

At each lithography scaling, the linear dimensions are approximately reduced by a factor of 0.7, and the areas are reduced by factor of 2. Smaller cell sizes lead to a higher integration density that has risen from 100 kilogates per mm^2 in the 130-nm technology to almost 1 million gates per mm^2 in the 45-nm technology. In parallel, the size of a six-transistor memory cell such

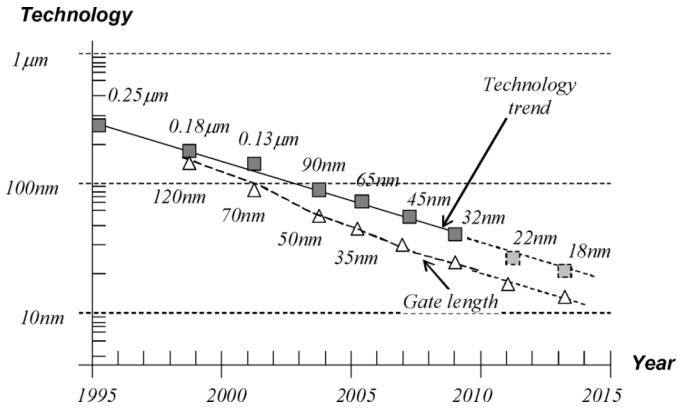

Fig. 2. The technology scale down toward nanoscale devices.

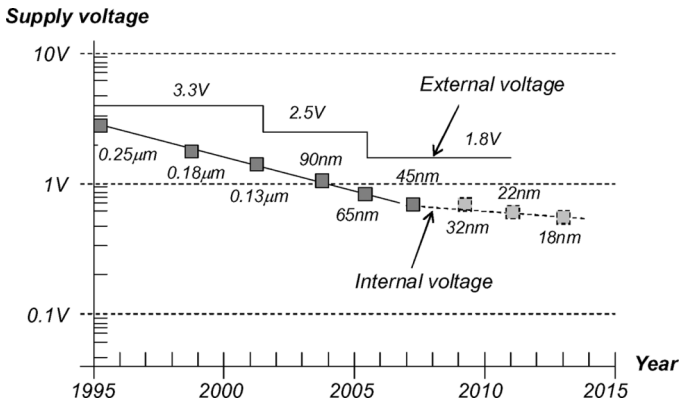

Fig. 3. The continuous decrease in supply voltage.

as those used in static RAM went below the 1-μm^2 limit after the introduction of 65-nm technology. The supply voltage tends to decrease (see Fig. 3) to reduce power consumption and limit the degradation mechanisms of the ultra-thin gate oxide. From 130 to 45 nm, the supply voltage has reduced from 1.5 to 0.9 V.

B. Improvements at Transistor Level

The channel length of MOS devices is automatically scaled with the technology. A scaling factor of 0.7 would lead to a

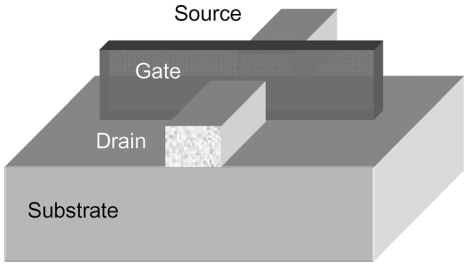

Fig. 4. The tri-gate concept proposed for 32- and 22-nm nodes [19], [20].

33% increase in the absolute current, with consequent increase in switching speed. However, the effective carrier mobility tends to degrade with a narrower channel. Two approaches have been introduced recently to improve transistor current capabilities further:

- Decreasing oxide thickness t_{OX}: The gate oxide thickness has been reduced to 1.2 nm (eight atoms) in the 90-nm technology. Unfortunately, the gate oxide leakage is exponentially increased, which increases the parasitic leakage currents and consequently the standby power consumption. For 40 years, polysilicon gates combined with SiO_2 (gate oxide) have been serving as the key enabling materials for MOS devices. Starting with the 45-nm generation, so-called "metal gates" have been introduced [1]–[4], based on nickel silicide (NiSi) or titanium nitride (TiN). In combination with high-permittivity dielectrics [14], [15] like hafnium oxide (HfO_2), the metal-gate transistors feature outstanding current-switching capabilities together with low leakage, as HfO_2 can be made much thicker than can SiO_2 for an equivalent gate capacitance effect. Increased ON current, decreased OFF current, and significantly decreased gate leakage are obtained with this novel combination. Future approaches should also include double- or triple-gate devices as illustrated in Fig. 4. Here, the gate controls the channel from three sides instead of one, which enhances capacitance effect and consequently switching properties.
- Increasing carrier mobility μ: This parameter was kept unchanged until the 90-nm generation. Starting with this generation, strained silicon has been introduced to enhance the carrier mobility [6]–[8], [17], [18], which boosts both the nMOS and pMOS transistor performances (Fig. 5).

III. Teaching Practices

A. A Review of Recent Educational Approaches

The never-ending shift toward nanoscale technology raises several questions about the educational approaches employed in IC design courses involving CMOS technology. Numerous intuitive approaches to facilitate students' understanding of microelectronic circuit fundamentals have been proposed in the past years. At the logic level, Hacker and Sitte [21] have presented an interactive teaching suite for the design of combinatorial and sequential logic circuits, while Tseng [22] has described an effective method of generating hardware implementation from various styles of procedural description. At the mixed-mode level, Hudson *et al.* [23] proposed an attractive sequence that includes digital, analog, and mixed-signal aspects of IC design. To help students overcome their fears of learning analog circuit design and handle the fast pace of the course, multiple hands-on learning experiences have been employed that allow the students to learn IC design using multiple modalities and observe real-world effects of ICs. The students have appreciated these hands-on experiences and have requested more throughout the sequence.

A review of fundamental low-power design techniques has been presented in [24], with examples to facilitate students' study and understanding. Switching time calculation has been specifically addressed by Kayssi [25], a topic covered in most VLSI courses. In the analog area, Mazhari [26] has proposed a representation of the differential amplifier that explicitly reveals the relationships between important amplifier specifications, and Corsi [27] has proposed an approach to analyze CMOS differential stages with active load. Karmalkar [28] has detailed the contents of a lecture for enhancing the interest of electrical engineering students in semiconductor device modeling, while Masters [29] created online animations for active learning of currents and fields in metal layers.

As for fabricating student designs, several relatively low-cost options have been available for accessing CMOS IC manufacturing, such as Europractice in Europe [30] or MOSIS in the USA [31]. However, the exponential increase in the costs of accessing nanoscale technologies in recent years and the steady increase in technology-driven design rules tend to limit the number of student projects sent to fabrication. Other issues include huge delay times in IC fabrication, the timelines for fabrication runs not matching the educational timetables, as well as assembly and testing efforts. In addition, as the number of hours dedicated to practical training with real silicon is gradually reduced, there is now a greater need for device-physics-related simulation tools so that students can still develop a deep understanding of designing with nanoscale technologies.

B. Challenges

First and foremost, it is acknowledged that the students need to develop as lifelong learners if they are to adapt to the rapid technological changes outlined in Section II and the consequent changes in design concepts and methodologies. In addition, it is necessary for them to develop the important graduate attributes of problem solving and critical thinking in order to operate successfully in a continually changing and challenging field of VLSI design. While it is important to ensure that the learning activities in the courses facilitate the development of up-to-date knowledge and industry-relevant design skills, it is equally important to ensure that the activities foster the development of the above-mentioned generic skills in an interesting and stimulating way. The challenge is how to accomplish this within the span of a semester that typically lasts for 13–14 weeks. Educators must be mindful of the following issues, which have the potential to render the task difficult unless due attention is paid right from the beginning:

- The commercial chip design tools available today are very powerful and are capable of meeting the design and verification needs of modern ICs. However, these tools are

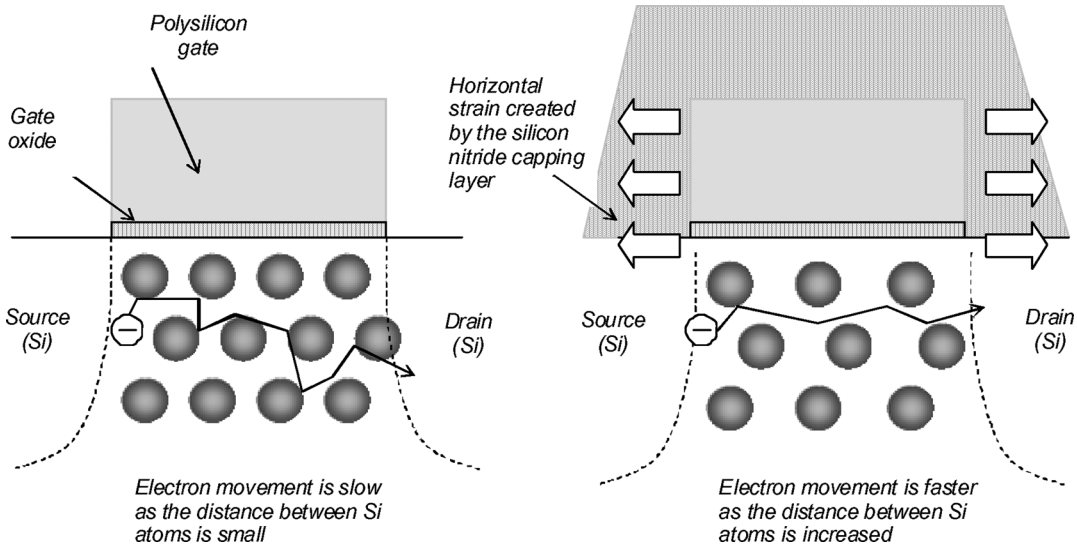

Fig. 5. Strain generated by a silicon nitride capping layer that increases the distance between atoms underneath the gate. This speeds up the electron mobility of n-channel MOS devices.

highly complex and take a long time to learn. If these commercial tools are used for student learning, the focus may unintentionally shift from developing actual technical knowledge and skills in circuit design to merely acquiring mastery of complex design tools.

- On the other hand, it is very important for students to develop a thorough understanding of the complex process technologies and their impacts on design alternatives using intuitive 2D/3D technology visualizations. Therefore, it is necessary to use design tools that are not only less time-consuming to learn, but also provide intuitive design, simulation, and visualization environments.
- The variation in background technical knowledge among the student cohorts presents another challenge [32]. From a pedagogical perspective, any gap in the background technical knowledge must be addressed first before effective learning of new concepts and skills can occur.

C. Teaching Context at UniSA, Australia

The UniSA course on VLSI design focuses on digital CMOS IC design. It is offered as a technical elective to final-year undergraduate students in four-year degree programs in Electronics and Microengineering, Computer Systems Engineering, Telecommunications, and Electrical and Mechatronic Engineering. It is also offered to students of Master's-by-coursework programs in relevant disciplines. Students are expected to have the necessary background knowledge and experience in digital logic design and electronics. The undergraduate students are expected to develop this background knowledge through compulsory courses on electronics and digital design in earlier years of their degree programs. However, the VLSI course is the first to introduce them to CMOS cell design. Also, the majority of the students who enrolled in the course in the last five years were from overseas, many of them pursuing Master's-by-coursework programs. These students come from diverse cultural, language, and educational backgrounds [33]. They possessed Bachelor's degrees in various branches of electrical, electronics, computer, and telecommunication engineering with different levels of exposure to the background knowledge and skills required to undertake the VLSI design course. This presented a challenge and required an inclusive learning environment for all students along with the use of user-friendly educational tools.

D. Teaching Context at INSA Toulouse, France

INSA offers a two-year program called *Master's in Automatic Control and Electronics*. In the first year of study, the students take a course titled *Physics and Modeling of Semiconductor Devices*. It consists of 20 h of lecture and 15 h of laboratory work. Due to the large number of students and the unavailability of student editions of professional computer-aided design (CAD) tools, educational tools are used, which cover the introductory logic and layout-level design in an interactive way. The training targets are basic CMOS cell design and simulation [34]. In the second year of the program, students attend 20 h of lecture in the course *Analog CMOS Circuit Design and Test*, including several aspects of advanced CMOS cell design [35]. Students also conduct a small VLSI design project equivalent to 20 h of practical work using educational design tools. However, the licensing requirements, cost, and the time needed to learn professional CAD tools can be justifiable in advanced (post-graduate level) courses and in research degree programs, as shown in Fig. 6, because of the limited number of students and in the interest of training future engineers in acquiring some knowledge of the complete industrial design flow. In the *Analog Circuit Design* course, the professional tools are only used to convert the students' layouts to industry format prior to fabrication because the educational tools cover a subset of the real process design rules.

IV. Proposed Design Flow and Software Tools

Most industrial CAD tools lack the ability to show the basic functionality and various aspects of CMOS circuits in an intuitive and graphical manner. What is important for student comprehension is the ability to act on a design, to define

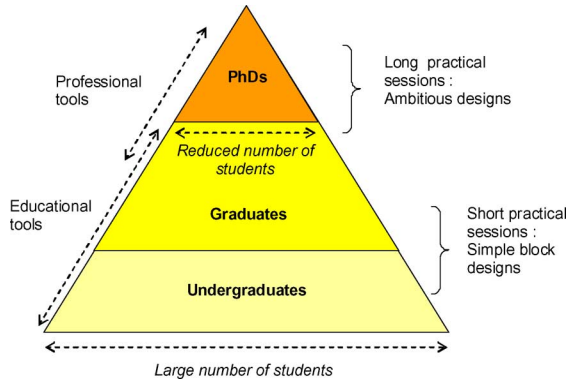

Fig. 6. Educational tools are mostly used for undergraduate teaching, while professional tools are used at Master's and doctorate levels.

intuitive test sequences, and immediately be able to view the electrical response. To fulfill these requirements, both UniSA and INSA mainly use a user-friendly layout-level design and simulation tool called *Microwind* [36]. To create layouts of large designs easily, a schematic-level design and simulation tool called *Dsch* is used [36]. These tools incorporate the most recent CMOS technologies and provide an interactive learning environment for the development of IC design and analysis skills. Another software called *WinSpice* [37] is used for the simulation of netlists generated from the layouts using various SPICE models incorporated within the *Microwind* tool.

A. Design Flow

The design flow used by students for the physical design of layout-level functional blocks is illustrated in Fig. 7. The tools *Dsch* and *Microwind* are used for creating schematic and layout level designs, respectively. Microwind's layout library (MOS generators, PAD generators, cell compiler) may be used to ease the design phase. The design rule checker is used to ensure compliance with technology constraints (minimum width, minimum distance between layers, etc.). Students also use the built-in analog simulator to verify that the functionality and performance comply with the specifications.

Once the layout is complete, a set of files is generated in a standard layout description format (CIF, GDS2 etc.) for transfer to a professional CAD environment. The reason why a professional layout tool is necessary prior to fabrication is that educational tools only verify a subset of the design rules. The final circuit is built by placing and connecting layout blocks and checking against the complete set of design rules.

B. Design Tools

This section briefly introduces the *Microwind* software, which emphasizes a user-friendly and intuitive design style for educational use. *Microwind* [36] is a CMOS circuit editor and simulation tool for layout-level design running on Microsoft Windows. It has developed through several versions since 1998 and is available as a freeware for educational purposes. In short, *Microwind* allows the student to draw the masks of the circuit layout and perform analog simulation. Some textbooks on CMOS design have been published around this software in the last few years [34], [35], [38].

The *Microwind* main screen, shown in Fig. 8, includes two windows: one for the main menu and the layout display, and the other for the icon menu and the layer palette. The main layout window features a grid scaled in lambda (λ) units. The lambda unit is fixed to half of the minimum available lithography of the technology in use, noted as $\mathrm{L_{min}}$. For example, the default technology is a CMOS six-metal layer 65-nm technology, and consequently lambda is 0.035 μm.

$$\lambda = \frac{\mathrm{L_{min}}}{2}. \tag{1}$$

From an educational viewpoint, the key advantages of the lambda-based system are:

- the ability to simulate the same layout with several technology files;
- the convenience of having to master only a single set of design rules (minimum gate length 2λ, minimum metal width 3λ, etc.).

C. Tutorial on MOS Design and Modeling

1) Traditional Approach: Students often tend to miss the essentials of device modeling even after extensive discussions of the mathematical approaches for several devices [28]. Modeling the MOS device consists of writing a set of equations that link the voltages and currents in order to simulate and predict the behavior of a single device and consequently the behavior of a complete circuit. Many books have been published about semiconductor physics and device modeling. The most common references used for education are [39] and [40]. Traditional teaching usually relies on an in-depth explanation of the potentials, fields, threshold voltage, and eventually the expression of the current Ids, which flows between the drain and the source, depending on the node voltages $\mathrm{V_d}$, $\mathrm{V_g}$, $\mathrm{V_s}$, and $\mathrm{V_b}$ as in (2) and illustrated in Fig. 9.

$$Ids = f(Vd, Vg, Vs, Vb). \tag{2}$$

2) New Approach: The approach presented in this paper is significantly different in that it aims at giving students immediate confidence to design MOS devices. The approach consists of a step-by-step illustration of the most important relationships between layout and performance.

Step 1–nMOS Layout: The students are asked to draw a MOS device using the layout interface shown in Fig. 8. Clicking and dragging the mouse adds polysilicon boxes on the layout. Students are then asked to change the active layer in the palette to add a diffusion box. This completes the design of the MOS device (Fig. 10). The students are then asked to perform a 2D cross section of the device. They observe the details of the layer structure (oxide, diffusion, gate) and how the gate splits the diffusion box into three regions—namely, the drain, channel, and the source (Fig. 11). At this stage, usual questions concern the color codes, the stack of oxides (as no metal is yet present), or the scale of the device.

Step 2–Electrical Performance: The students are invited to evaluate the static electrical performance of the device. An icon gives access to the $\mathrm{I_d/V_d}$ curve, which is plotted for varying gate voltage $\mathrm{V_{gs}}$, from 0 to $\mathrm{V_{DD}}$ (Fig. 12). It enables students to act on the operating point in the $\mathrm{I_d/V_d}$ curve. Students are asked

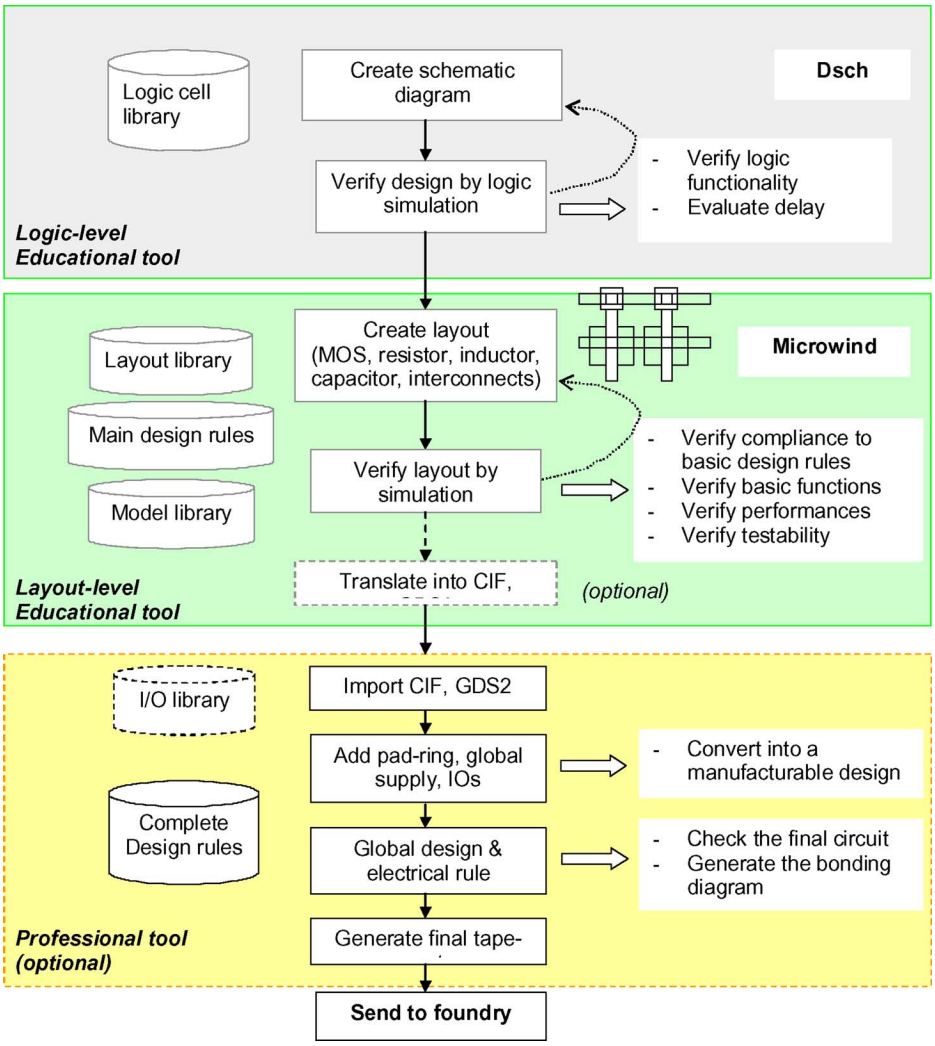

Fig. 7. Design flow for teaching concepts of CMOS cell design.

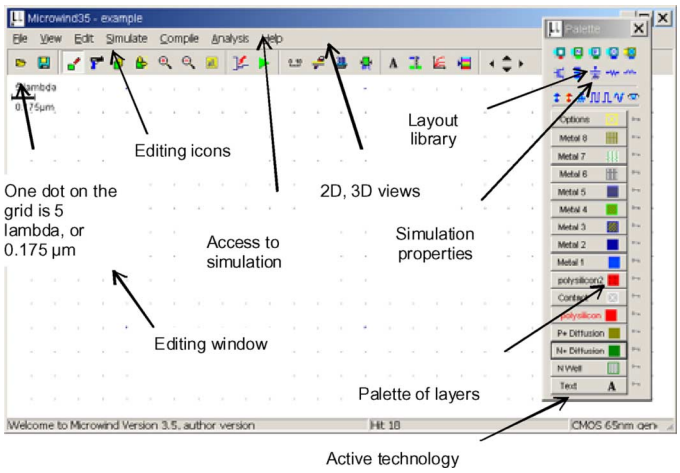

Fig. 8. The MICROWIND screen as it appears at the initialization stage.

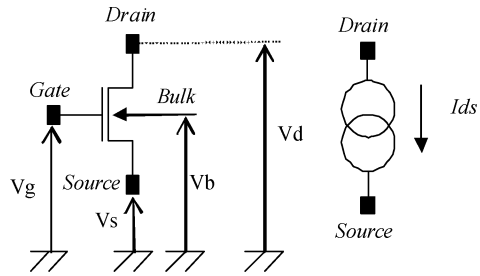

Fig. 9. Symbolic representations of the MOS device.

to extract Ion, which gives an important indication about the maximum available current. As MOS designs differ from one student to another, waveforms and values are not identical. Once the functional point is placed at Ion (after some search), with for example $\mathrm{Vg} = 0$, $\mathrm{V_d} = \mathrm{V_{DD}}$ and $\mathrm{Vg} = \mathrm{V_{DD}}$, the concept of voltage control and first-order impact on current becomes obvious to students.

In *Microwind*, three important generations of device models are accessible from a single interface window: MOS model 1 [41], LEVEL 3 model [42], and BSIM4 model [43]. The number of parameters specified in the official release of BSIM4 is as high as 500. A large number of these parameters are not important in early teaching phases. The concentration in this step, therefore, is on those parameters that are most significant for

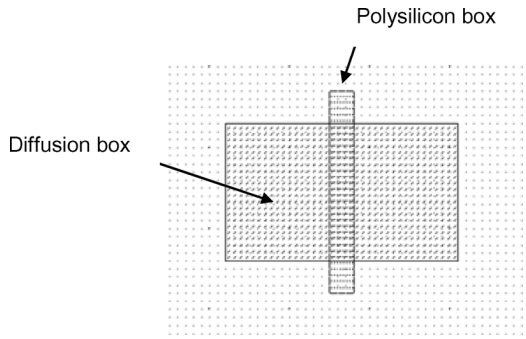

Fig. 10. The first MOS device designed by the student.

educational purposes. For example, in *Microwind*, the set of user-accessible parameters is reduced to around 30 for BSIM4.

Step 3–Interactive Simulation of the Layout: The students use a set of simulation properties (clocks, pulses, dc voltage sources) to build a test scenario to validate the concept of a voltage switch controlled by a gate voltage. A usual approach followed by students consists of placing clocks on the gate and drain and then monitoring the source (Fig. 13). This leads to the timing diagrams of Fig. 14, which stimulate students' thoughts on the factors influencing the performance of the MOS device. Through careful investigation of the simulations, students are able to gather information about the key properties and drawbacks—for example, junction capacitance effect that samples undesired intermediate voltage, threshold effect that jeopardizes the high voltage levels, and ultrafast charge/discharge (in picoseconds range).

Step 4–pMOS Layout: Students are then asked to build a pMOS device and observe the complementary behavior. The training also includes inverter design and analysis of sizing effects on static transfer characteristics. Finally, the students are asked to copy/paste several inverters and build interconnects to construct a ring oscillator, as in Fig. 15, which has the property of oscillating naturally.

Step 5–Simulation of the Ring Oscillator: Students simulate the ring oscillator layout using various technologies in *Microwind*. The desired technology is chosen simply by selecting the corresponding *rules file* using the *foundry command* under the *file menu*. The time-domain waveforms of the outputs are shown in Fig. 16 for 0.8-μm, 0.18-μm, and 45-nm technologies. Students are able to visualize and analyze the impacts of technology scaling. Although the supply voltage (V_{DD}) has been reduced with technology scaling (5 V in 0.8 μm, 2 V in 0.18 μm, and 1.0 V in 45 nm) the gain in frequency improvement is significant. A contest is usually organized to obtain the fastest oscillating frequency, which involves several aspects of layout optimization, such as minimum gate length, suppression of spared diffusion areas, minimum distance between inverters, and so on.

V. Project-Based Learning

PBL methods have been developed for the courses at both UniSA and INSA. In both cases, the aim is to engage students in a stimulating learning experience for the development of professional design skills using the latest semiconductor technologies and for the development of independent and lifelong learning abilities. The issue of student diversity is addressed in UniSA by following a structured project-based approach. At INSA, a similar approach is adopted for the introductory course on *Physics and Modeling of Semiconductor Devices*. However, a more open-ended approach is adopted in the course on *Analog CMOS Circuit Design*.

In the structured PBL methodology, the students do simple projects in the early stages of the course using step-by-step *self-learning guides*. Critical questions and increasingly complex tasks are gradually scaffolded within the projects. These questions and tasks are aimed at stimulating students' curiosity and thinking, thereby engaging them to carry out their own investigations [44]. The early projects, done mostly in a self-learning manner, assist students in

- reviewing and/or developing the necessary fundamental concepts;
- learning how to use the design tools;
- developing problem-solving and critical-thinking skills;
- developing independent learning skills.

Students who possess relatively advanced levels of background technical knowledge can progress through the projects at their own (often faster) pace. On completion of each of the early projects, the students get the satisfaction of having designed a circuit that performs some useful function. This is useful for confidence building and motivation, particularly for the students who are new to the idea of independent learning and whose previous educational experiences may have been quite different from the engaging PBL approach. The remainder of this section gives an overview of the projects used in the PBL approach in two institutions, followed by a general discussion.

A. UniSA

As stated previously, the UniSA course on VLSI design uses simple self-learning projects at the beginning. The projects gradually increase in complexity, requiring students to engage in deeper problem solving and critical thinking. Finally, there is a capstone project on designing a microprocessor that challenges students by putting the knowledge and skills they have developed to test. Students do a total of six projects, which are briefly described below. They complete these projects mostly within the 2 h of the weekly laboratory session over a 12-week period.

1) First Two Projects–Circuit Analysis and Optimization Using WinSpice: The first two projects allow students to develop practical experience in circuit analysis and optimization using *WinSpice* [37], a version of the well-known Simulation Program with Integrated Circuit Emphasis (SPICE). While the first project handout guides the students through the simulation and optimization of a simple inverter circuit, it asks students a number of critical questions along the way, which require them to reflect on the work they do and results they obtain. The questions highlight the impacts of various MOS model parameters and of the device geometry on critical performance parameters such as propagation delay, switching characteristics, noise margin, dynamic power dissipation, and the like. The second project requires students to model a long transmission line driven by an inverter and to simulate it using the experience

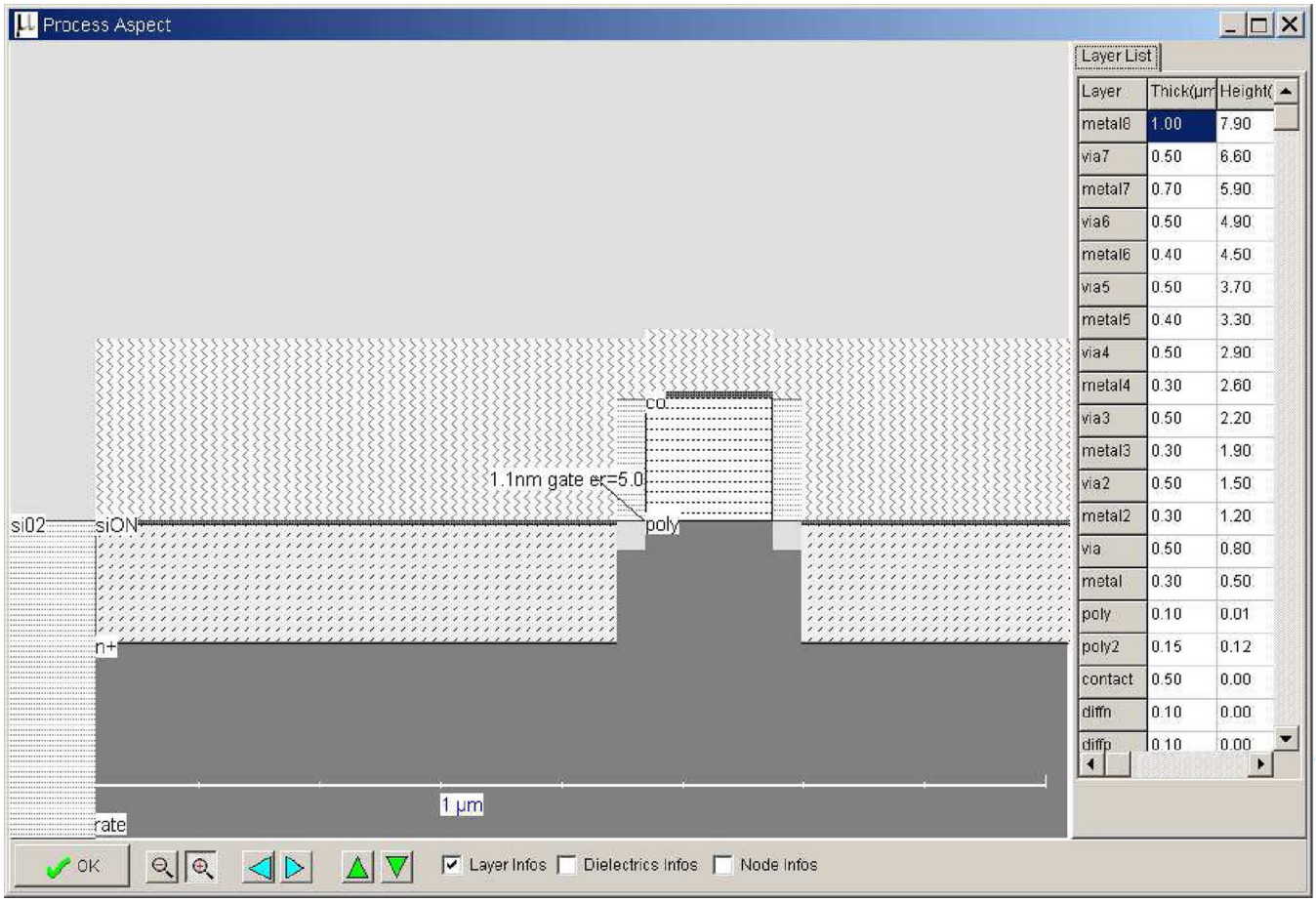

Fig. 11. 2D cross section of the MOS device.

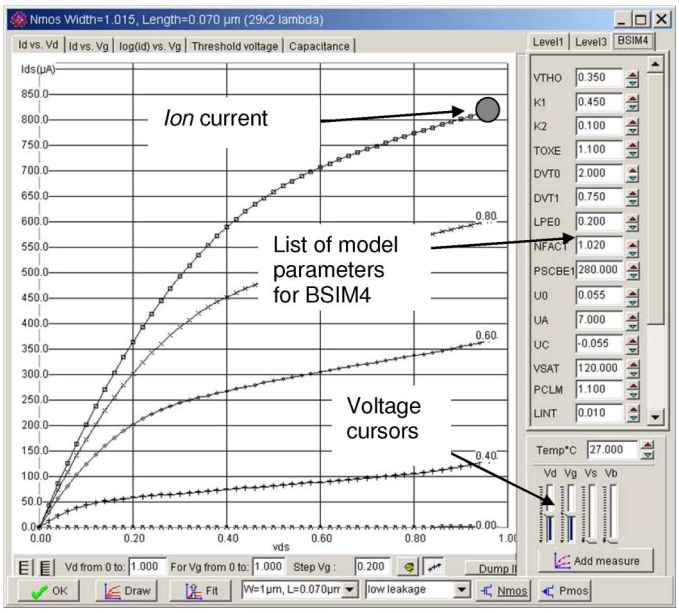

Fig. 12. Performance of the MOS device with user accessible parameters.

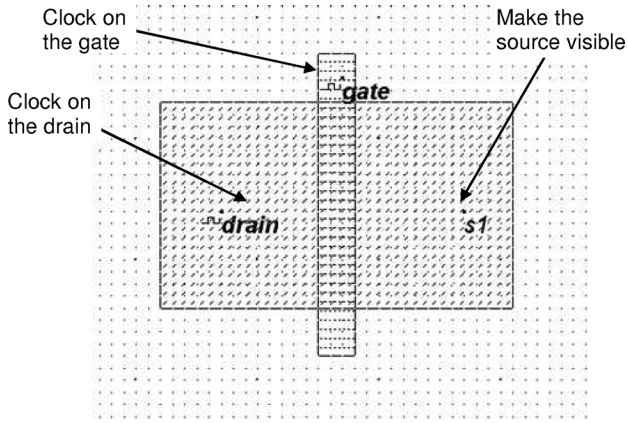

Fig. 13. MOS layout simulation.

they gained from the first project. They are required to examine the effects of the transmission line on signal quality and propagation delay. They develop useful insights by examining mechanisms to deal with these performance issues. In this project, the students also develop practical experience on the effects of stacked and parallel transistors on the performance of logic gates.

2) Project 3 and 4–Combinational and Sequential Circuit Layouts: In the third and fourth projects, the students develop practical experience in designing simple combinational cell layouts and clocked sequential circuit layouts using a structured cell-based design methodology. They perform DRC and simulation on the created layouts. They also perform various tradeoffs in relation to device geometry, layout area, and performance. In

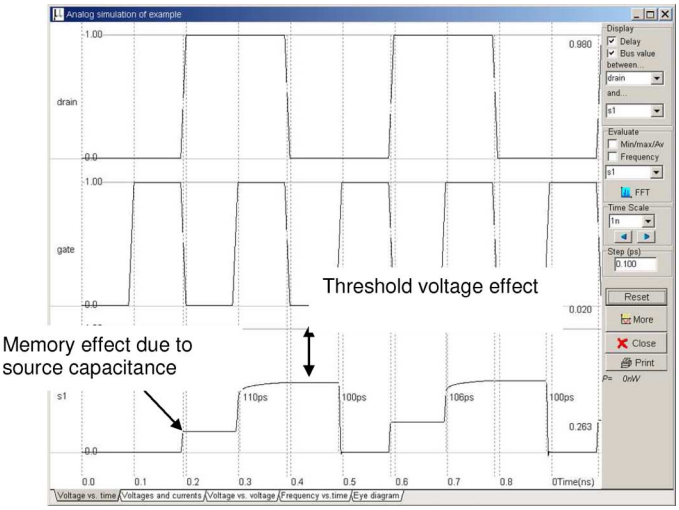

Fig. 14. Typical time-domain waveforms of the gate, drain, and source voltages obtained by analog simulation.

the fourth project, students automatically generate a 4-bit dynamic shift register layout in *Microwind* using a 1-bit inverting dynamic shift register cell layout they create manually. Students develop practical experience with two-phase nonoverlapping clocks by simulating the 4-bit register using the built-in simulator. Fig. 17 shows the layout of the 4-bit dynamic shift register.

3) Project 5–ALU Design: In the fifth project, students design an arithmetic unit using a schematic design tool called *Dsch* and verify its functionality through simulation. They then automatically generate a Verilog description using the *Make Verilog File* command in the *File* menu. Finally, they generate a layout in their chosen technology using the *Compile Verilog File* command in the *Compile* menu of the Microwind tool. Both Dsch and Microwind have the same range of technology rules files available. Therefore, the layout compiled in Microwind is implemented in the same technology as used in the original schematic design.

4) Project 6–Capstone Project on Processor Design: The final project challenges students to put their design skills into practice by designing a microprocessor with embedded static RAM, verifying the functionality through simulation, generating layout, and performing DRC. Students follow a hierarchical cell-based design method using *Dsch*. They generate a Verilog description of the processor and compile this in *Microwind* to generate the layout. Students aiming to achieve higher goals are inspired to conduct layout simulation or enhance the processor by incorporating additional instructions. Here, the students gain valuable experience on the challenges involved in simulating large IC layouts and explore alternative solutions.

B. INSA

This section gives an overview of two projects conducted by INSA students in the course *Analog CMOS Circuit Design*. After 6 h of tutorial on designing basic blocs (see Section IV-C), students have about 14 h to complete a project of their choice, examples of which include a rail-to-rail amplifier, a power amplifier for Bluetooth, RAM, ALU, a basic FPGA bloc, and a DSP multiply and accumulate block.

1) Project 1–Push–Pull Amplifier: The students are given schematic diagrams of conventional CMOS amplifiers. They try to implement these circuits on their own and optimize the layouts to satisfy predefined constraints linked to specifications such as operating voltage range or dc consumption at cutoff frequency. The push–pull amplifier shown in Fig. 18 is built using a voltage comparator and a power output stage. The difference between Vp and Vm is amplified and produces a result, $Vout$. Transistors *Nb* and *Pb* are connected as diodes in series to create an appropriate voltage reference V_{bias}, fixed between the nMOS threshold voltage Vtn and half of $\mathrm{V_{DD}}$. The differential pair consists of transistors *N1* and *N2*. Three stages of current mirrors are used: *P1/P2*, *P3/PO, N4/NO*. The output stage consists of transistors *PO* and *NO*. These transistors are designed with large widths in order to lower the output resistance. Such a design is justified when a high current drive is required. An example of a student design and its simulation are shown in Fig. 19(a) and (b), respectively. A lot of care has been taken to match device sizes and limit the silicon area.

The transient simulation of Fig. 19(b) shows some oscillation at the output, which denotes an output stage drive improperly matched to the load. Virtual capacitors may be added directly to the layout to emulate the realistic loading conditions. Students are also asked to produce dc transfer characteristics to characterize the valid input range for their amplifier. Reference books such as [35] are given to the students to investigate more complex circuits.

2) Project 2–Power Amplifier: CMOS power amplifiers, as shown in Fig. 20, used in radio-frequency output stages (such as Bluetooth of WiFi) require a very large current drive, which can be achieved with MOS devices in parallel. Students are asked to design MOS devices with Ion drive such as 100, 250, or 500 mA. As illustrated in Fig. 20(b), the metal supply must be designed with care to handle such large currents. At the start, the L, R, and C elements are added through virtual symbols for simplicity's sake. Again, the dynamic plot of the functional point is one attractive way to illustrate the concept of amplifier classes. For example, Fig. 21 corresponds to a Class A regime, where the functional point is always in the linear domain. Combining on-chip inductors and capacitors results in resonant systems that are tuned to the specified wireless system. For example, the integrated 3-nH inductor with 1.5 pF capacitance produces a resonance around 2.4 GHz.

C. Discussion

Through the different projects, the students visualize how the two design tools *Dsch* and *Microwind* can be used to design complex integrated circuits using the latest semiconductor technology. After 2 h of practice, the students fairly readily develop competence in using the tools. 2D cross sections and 3D-animated views in *Microwind* are extremely useful for students to visualize how the IC is built using different layers and their interconnections and the potential sources of errors, for example, missing interconnects between layers. Students develop design skills at layout level, are able to optimize the layout to increase

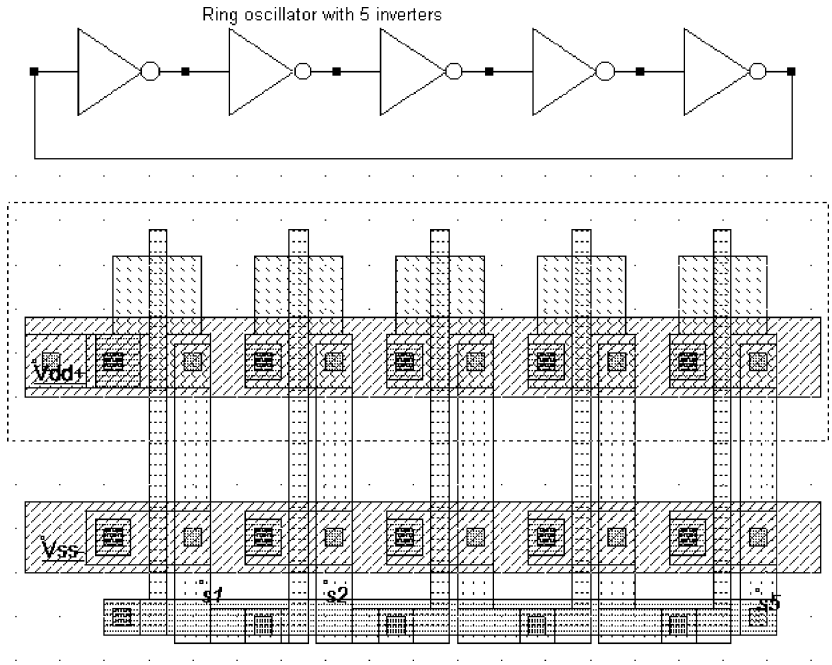

Fig. 15. Schematic diagram and layout of the ring oscillator used for simulation.

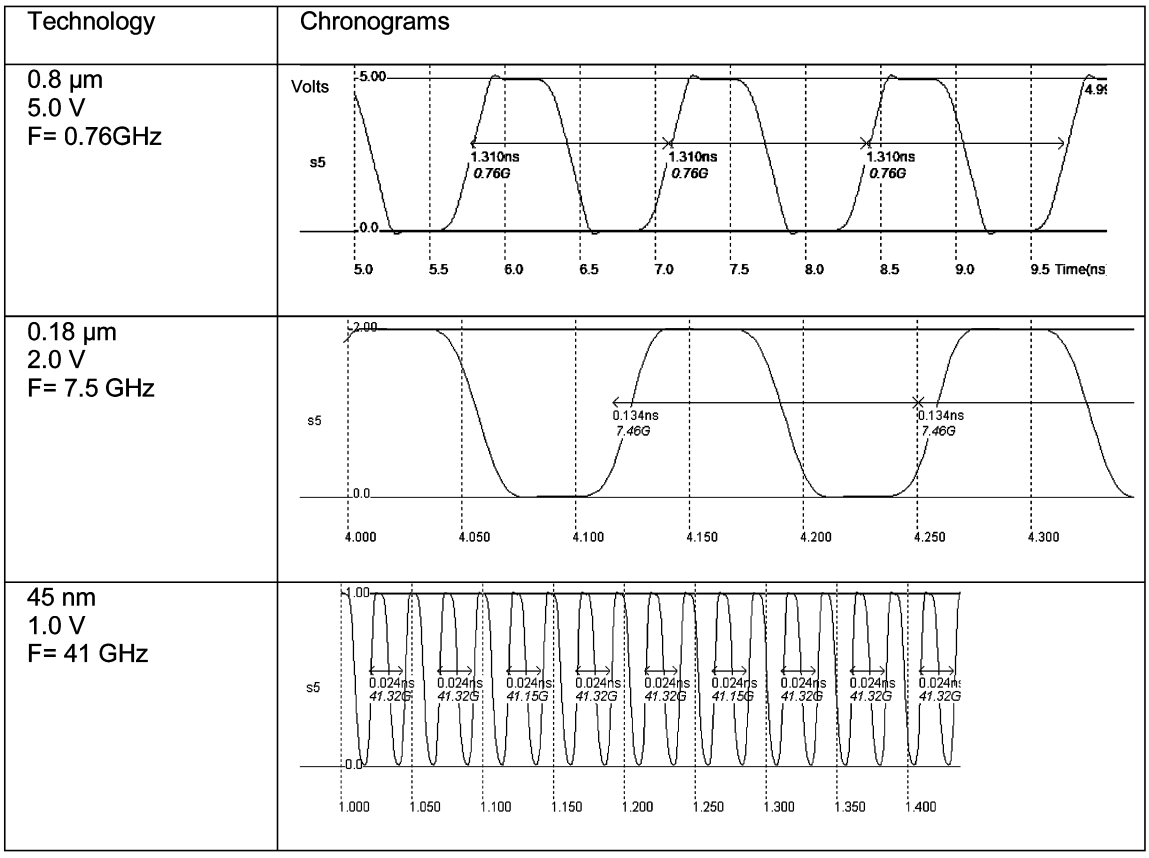

Fig. 16. Oscillation frequency improvement with technology scale down.

speed, reduce the silicon area, and check the layout for DRC. Students also acquire useful experience on the effects of device sizing and realize the efficiency of automatic layout generation from high-level description. They gain experience in the challenges involved in designing and simulating complex ICs and are ready to explore professional tools and the most recent models [45] available to industry. The proposed PBL methodology can be used with commercial design tools, however the learning times of these tools are normally quite high. This means less time can be devoted to developing actual circuit design skills. The commercial tools do not normally provide intuitive 2D cross sections and 3D animated layout views, nor do they

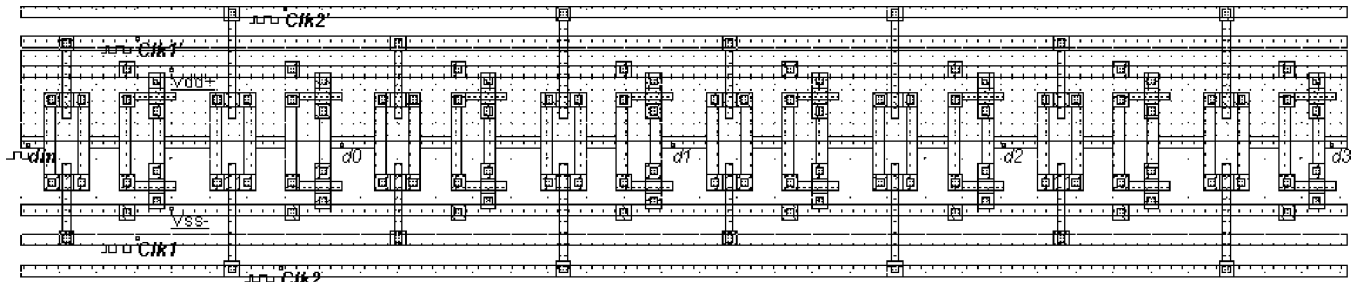

Fig. 17. Four-bit dynamic shift register layout.

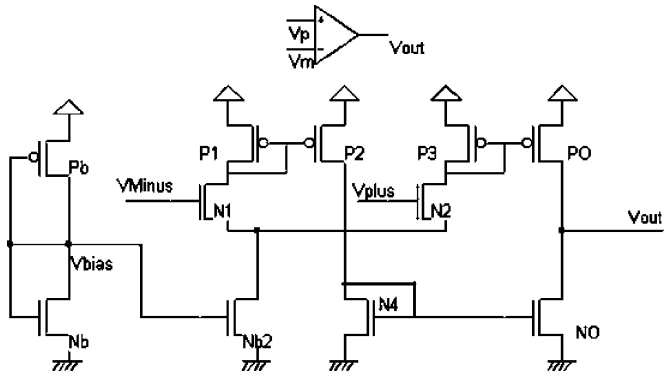

Fig. 18. Schematic diagram of a push-pull operational amplifier.

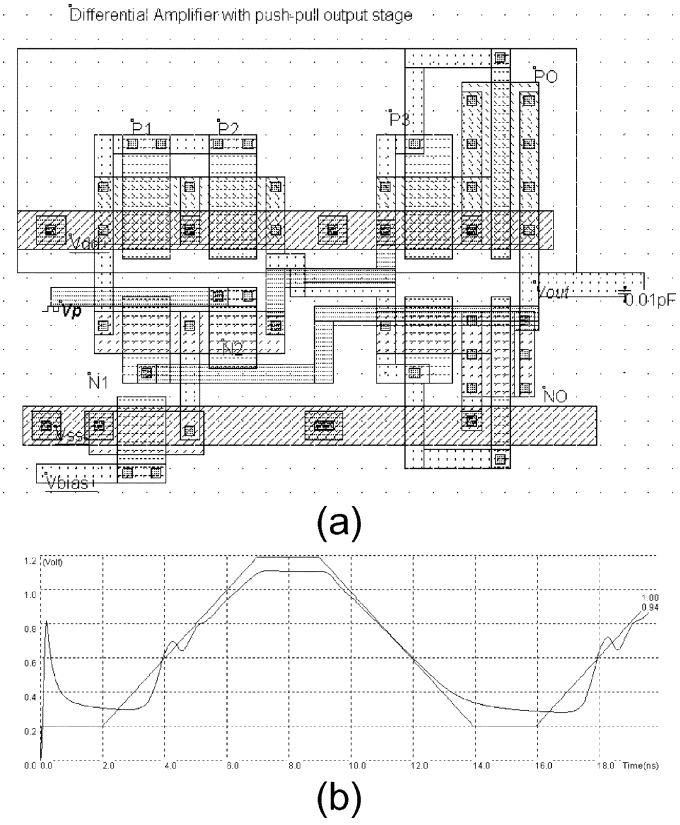

Fig. 19. (a) Layout and (b) time-domain simulation of a push–pull operational amplifier connected as a follower.

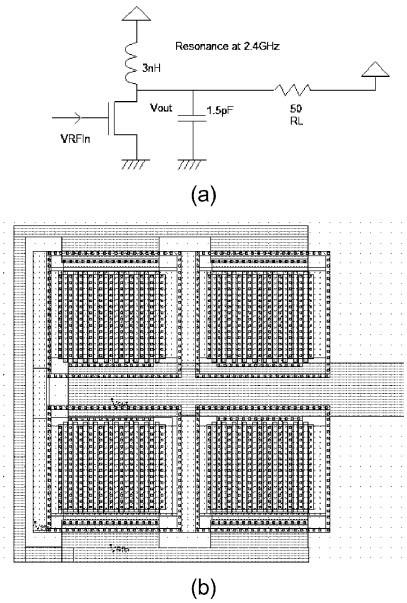

Fig. 20. (a) Schematic diagram of a power amplifier and (b) MOS layout featuring 250 mA Ion drive.

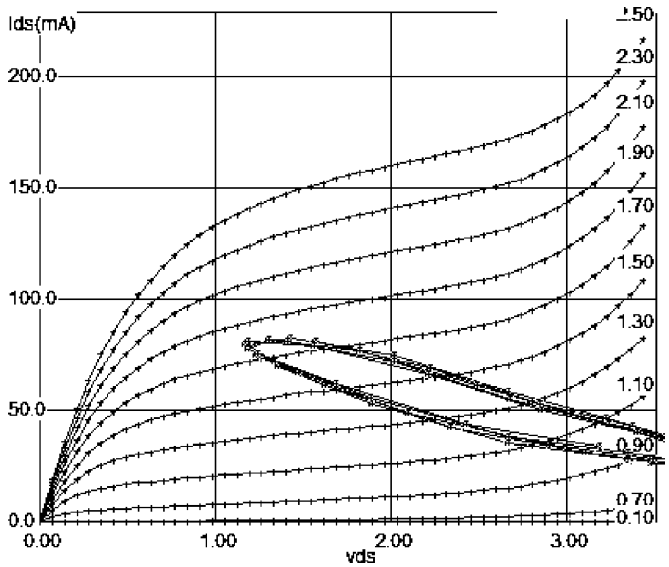

Fig. 21. Illustration of the Class A amplification in the I/V curve of the power MOS.

incorporate simplified SPICE models for quick visualization of the impacts of important model parameters on device or circuit performance using intuitive interfaces. These are the reasons why the educational tools proposed here are better suited to teaching IC design compared to commercial IC design tools.

TABLE II
COURSE EVALUATION QUESTIONNAIRE

#	Question
1	I have a clear idea of what is expected of me in this course.
2	The ways in which I was taught provided me with opportunities to pursue my own learning.
3	The course enabled me to develop and/or strengthen a number of the qualities of a University of South Australia graduate.
4	I felt there was a genuine interest in my learning needs and progress.
5	The course developed my understanding of concepts and principles.
6	The workload for this course was reasonable given my other study commitments.
7	I have received feedback that is constructive and helpful.
8	The assessment tasks were related to the qualities of a University of South Australia graduate.
9	The staff teaching in this course showed a genuine interest in their teaching.
10	Overall I was satisfied with the quality of this course.

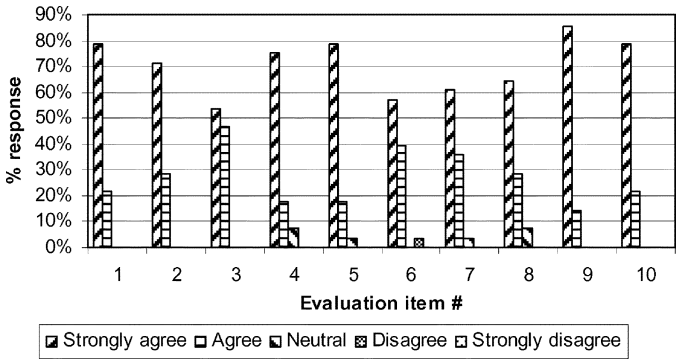

Fig. 22. 2006 course evaluation responses at UniSA.

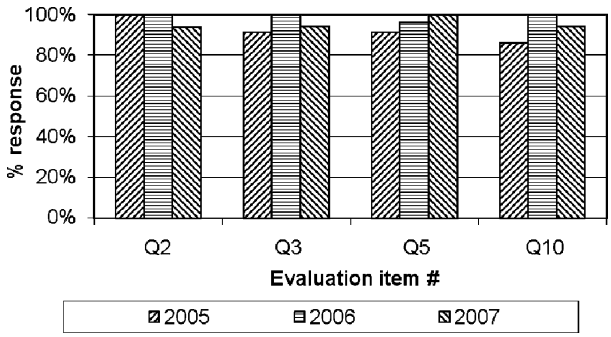

Fig. 23. Responses to four key evaluation items for three consecutive years.

VI. EVALUATION

This section provides a summary of student experience in the two institutions. Responses to anonymous course evaluation questionnaire and special questionnaire on PBL are included.

A. UniSA Student Evaluation

The VLSI course was evaluated anonymously by the students using UniSA's standard course evaluation questionnaire containing 10 core questions and some open-text response questions. The core evaluation items are presented in Table II. Students select a response to each statement from a Likert scale of 1 to 5, where a score of 5 signifies strong agreement with the statement and 1 indicates strong disagreement. Fig. 22 presents the student responses to the questionnaire in the year 2006. Clearly, the students rated the course very highly in all the evaluation items. The course achieved similar high rankings in successive years since 2005 and was placed in the top quartile among the courses offered in engineering and IT disciplines in UniSA. The rankings achieved by the course in many of the evaluation items were the highest among the UniSA courses. Fig. 23 presents student responses to four key evaluation items (2, 3, 5, and 10 in Table II) for three consecutive years.

It is clear from Fig. 23 that the course consistently achieved very high levels of student satisfaction in these areas. The intuitive design tools and the PBL methodology along with the self-learning project guides contributed toward the achievement of such positive outcomes. Some representative comments from the students about the course are given:

> "[The VLSI design course] gives the students a very good exposure to the up-to-date CMOS technology. It's a specialist course."

> "Quality of practical handouts is great. Material covered is highly relevant and useful. Teaching is of an exceptionally high quality."

The various strategies used in the PBL approach were also anonymously evaluated by the students. The questionnaire developed for this purpose in consultation with advisers in UniSA's Learning and Teaching Unit (LTU) is given in Table III. The Likert scale responses are given in Fig. 24. Clearly, the students found the PBL approach very useful for their learning. In one student's view:

> "The project-based learning was very good, the first project had in-depth instructions and it gradually backed

TABLE III
QUESTIONNAIRE FOR EVALUATION OF THE PBL APPROACH AT UNISA

#	Question
1	I was able to work out how to use the CAD software by using the project handouts provided
2	I was able to learn circuit design techniques on my own by doing the projects using the project handouts
3	The handouts assisted in revisiting some of the background knowledge required for the course
4	The questions given in the project handouts helped me to think critically
5	The projects helped me put the theory of VLSI Design into practice
6	The final capstone project challenged me to test my learning in the course
7	I feel confident about completing similar capstone projects independently
8	The skills I learn in VLSI project work are useful to me
9	Overall I am satisfied with the project-based learning approach used in the VLSI Design course

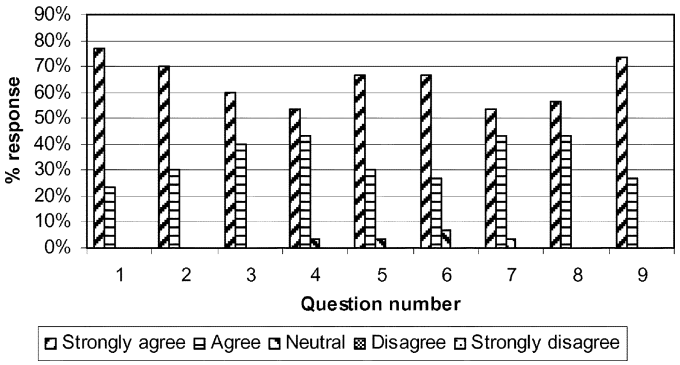

Fig. 24. Student responses to evaluation of the PBL approach.

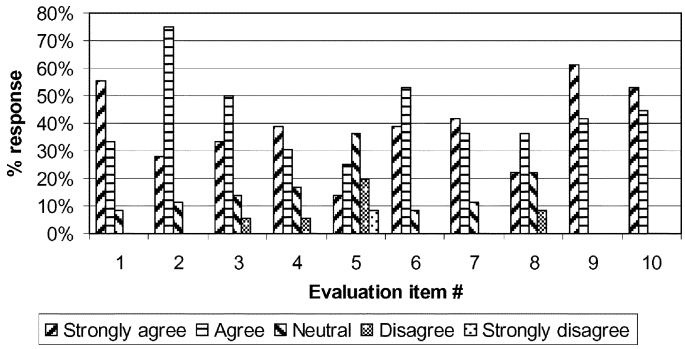

Fig. 25. 2007 course evaluation responses at INSA.

off, giving us time to adapt to the software and applying the theory."

B. INSA Student Evaluation

The questionnaire of Table II was also used at INSA for anonymous evaluation of the course *Analog CMOS Circuit Design* during two sessions in October 2007. The student responses are shown in Fig. 25. All respondents said that they were satisfied with the overall quality of the course (55% strongly agree, 45% agree). This is comparable to the UniSA results of Figs. 22 and 23. The feedback from students in 2008 were very similar to those in 2007. However, in response to item 5, some INSA students highlighted some mismatch between the theoretical part of the course, mostly related to the physics of devices, and the practical part, oriented toward layout design.

Some representative comments from the students about various aspects of PBL and the educational approach are given:

"From just a few logic gates, we have created a 4-stage binary counter which is ready to be fabricated on a silicon wafer. It also gave us the basic concepts to understand the operation of the transistors in order to extract their models and to use them in complex analog or digital circuits."

"The 24-h clock project was a good exercise which permitted us to see how it is inside a semiconductor and how it works."

"Throughout this project, we learned a lot about designing an integrated circuit. We learned basic design rules and we could apply these rules in a small project. We faced some practical problems, shown by the simulation, and we tried to solve them or to understand them."

"This study allows us to understand the function of a DAC. In spite of some design problems, we managed to make the DAC work well."

"Before doing this project, we hadn't thought that there were so many ways to design an amplifier. It's an area not easy to understand. Each technique has its limit. We tried to optimize our operational amplifier design to maximize the gain."

C. Peer Evaluation

Evaluation versions of the design tools *Microwind* and *Dsch*, along with the user manuals and the software application notes for various nanoscale technology nodes, are available online at http://www.microwind.org/. This Web site also contains links to the student project site containing reports on various projects undertaken by the students at INSA. These documents can also be found at http://www.microwind.org/docs.html along with some additional resources. The UniSA project resources are available online at http://tiny.cc/UniSAVLSI. Interested instructors can obtain further information by contacting the authors directly. The design tools (*Microwind* and *Dsch*) are used for educational purposes by almost 500 institutions worldwide, including North America, Europe, Asia, and Australia. In India alone, there are more than 200 educational institutions using full licensed versions of the above design tools. This has enabled the authors to obtain valuable feedback on various aspects of the design tools, nanometer technology models, and course resources on an ongoing basis. Many academics have been acting as beta testers of the design tools. The critical feedback obtained from the instructors and students worldwide have enabled continuing improvement and refinement of the tools and learning resources. Some representative comments from the academics are given:

> "The *Microwind* and *Dsch* tools along with the project-based course resources have assisted us greatly to enhance our educational program in Microelectronics within our Bachelor of Engineering degree. The tools offer easy to use menus for design and simulation, and the choice of a range of intuitive technology models to enable students to develop critical design and analysis skills using the latest technologies."—A. K. Halim, Lecturer, Universiti Teknologi Mara (UiTM), Shah Alam, Malaysia.

> "Teaching integrated circuit design commenced at our university in 1995 using the *Microwind* and *Dsch* tools. Since then the tools have undergone phenomenal development focusing primarily on enhancing students' learning experience through provisioning of latest CMOS technologies, simplified device models and powerful visualization interfaces. These tools and the supporting learning resources developed at INSA and UniSA are being used in a number of universities in Bangladesh. The PBL approach fostered by the learning resources stimulates students to develop advanced circuit design, modeling, simulation, and analysis skills in a self-learning manner."—A. B. M. Harun-ur Rashid, Professor, Bangladesh University of Engineering and Technology, Dhaka, Bangladesh.

> "The *Microwind* and *Dsch* programs are extremely powerful tools, and exploring them was a lot of fun. The interface is very friendly, and the program is both educational and useful for designing CMOS chips."—Late J. P. Uyemura, Professor, Georgia Institute of Technology, Atlanta [38].

VII. Conclusion

The use of intuitive and user-friendly design tools that enable students to develop circuit design skills using modern deep submicron technology has been one of the underlying factors for the successful delivery of the digital and analog IC design courses in two institutions in Australia and France. The sharing of experience and the collaborative development of tools and resources have contributed toward deploying effective PBL methodologies for teaching IC design. Engaging students in design work involving a range of the latest technologies has enabled them to understand the impacts of technology scale down on factors such as speed, power, and noise. The important areas of modeling and simulation are covered through the use of simplified SPICE models for the deep submicron technologies. Using project-based learning methodologies suited to the teaching contexts, digital and analog circuit design courses have been delivered with high levels of student satisfaction. The philosophies behind this approach have been responsiveness to the teaching context and student diversity in particular, emphasis on the development of circuit design concepts and skills rather than mastery of complex design tools, and projects that are able to stimulate student curiosity and thinking. The project-based methodology may need some adjustments based on the students' background and experience. The authors believe that these resources, tools, and the PBL methodologies will be useful for teaching VLSI cell design in different contexts and for developing the students' technical design skills as well as the soft skills of critical thinking and lifelong learning, which are crucial in the rapidly changing field of microelectronic circuit design.

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